LISTING OF CLAIMS

Please **AMEND** claims 2, 3, 12 and 18 as follows.

A copy of all pending claims and a status of the claims is provided below.

1. (original) A method for testing an electronic circuit, comprising:

defining a first initial vector;

defining at least one segment within the first initial vector;

offsetting the first initial vector a predetermined amount within the at least one segment;

defining a counter loop comprising loops of the first initial vector within the at least one segment to produce a first set of vectors in accordance with the counter loop;

defining a progressively changing variation of the first initial vector for each loop of the counter loop so at least one vector of the first set of vectors varies from the first initial vector; and

coupling the at least one segment having the first set of vectors including the varied at least one vector to produce a final pattern for a circuit under test.

2. (currently amended) The method of claim 1, wherein defining a the first initial vector comprises selecting a predefined vector pattern.

3. (currently amended) The method of claim 2, wherein defining a the first initial vector further comprises at least one of running a vector, delaying a vector, rerunning a vector, and looping a vector.

4. (original) The method of claim 1, further comprising overriding the first initial vector with a second vector.

5. (original) The method of claim 1, further comprising selecting an input pin on a device to be tested for the first initial vector.

6. (original) The method of claim 5, further comprising defining a name for the input pin on the device to be tested.

7. (original) The method of claim 1, further comprising defining a counter, and looping the first initial vector a prescribed number of times in accordance with the counter.

8. (original) The method of claim 1, further comprising defining a data control vector to allow a prescribed input format of the first initial vector.

9. (original) The method of claim 1, further comprising defining a new format vector to be added to the first initial vector to reconfigure the shape of the first vector.

10. (original) The method of claim 1, further comprising:

defining a second vector;

allocating a second segment configured to contain the second vector; and

offsetting the second vector a predetermined amount within the second segment.

11. (original) The method of claim 10, further comprising:

defining a counter loop comprising loops of the second vector within the second segment to produce a second set of vectors having a prescribed number of vectors in accordance with the counter loop;

defining a progressively changing variation of the second vector for each loop of the counter loop so at least one vector of the second set of vectors varies from the second vector; and

outputting the second segment having the second set of vectors.

12. (currently amended) A method of generating a test pattern, comprising:

selecting a macro definition file defining at least one vector;

forming a control bit definition file configured to be added to the at least one vector;

creating a pattern definition file configured to selectively alter a portion of the at least one vector;

creating a global definition file configured to alter the entire vector; and

combining the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern.

13. (original) The method of claim 12, further comprising repeating the final pattern in accordance with a counter range.

14. (original) The method of claim 12, further comprising forming setup vector files configured to power-up a device under test.

15. (original) The method of claim 12, further comprising forming stability vectors files configured to stabilize a device under test between actual test signals.

16. (original) The method of claim 12, further comprising outputting the final pattern to a device under test.

17. (original) The method of claim 12, further comprising creating multiple final patterns and adding the multiple final patterns to one another.

18. (currently amended) The method of claim 17, further comprising at least one of ~~any one of~~ overlapping, delaying, mixing, and offsetting at least two of the multiple final patterns.

19. (original) A computer program product comprising a computer usable medium having readable program code embodied in the medium, the computer program product including at least one program code to:

define a first initial vector;

define at least one segment within the first initial vector;

offset the first initial vector a predetermined amount within the at least one segment;

define a counter loop comprising loops of the first initial vector within the at least one segment to produce a first set of vectors in accordance with the counter loop;

define a progressively changing variation of the first initial vector for each loop of the counter loop so at least one vector of the first set of vectors varies from the first initial vector; and

coupling the at least one segment having the first set of vectors including the varied at least one vector to produce a final pattern for a circuit under test.